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10/669,308	09/23/2003	Bin Wan	REAP0495USA	3921

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EXAMINER	
AHMED, ENAM	

ART UNIT	PAPER NUMBER
2112	

NOTIFICATION DATE	DELIVERY MODE
11/27/2007	ELECTRONIC

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Notice of the Office communication was sent electronically on above-indicated "Notification Date" to the following e-mail address(es):

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Office Action Summary	Application No.	Applicant(s)	
	10/669,308	WAN ET AL.	
	Examiner	Art Unit	
	Enam Ahmed	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 September 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-22* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *11/22/06 and 12/23/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Final Rejection

This office action is in response to Applicants Amendments of 18 September 2007.

Claims 1 and 19-22 have been amended.

Claims 1-22 remain pending.

The prior art rejections of record are maintained in response to applicants amendment of 9/18/07.

The objection to the specification is withdrawn.

The objection to the abstract of the disclosure is withdrawn.

The objection to the claims has been withdrawn.

The rejections under 35 U.S.C. 101 have been withdrawn.

Response to Arguments

Applicants arguments of 9/18/07 have been fully considered, and are not found persuasive.

Response to Applicants Remarks

On page 13, the applicants state that Delvaux's interleaver uses only a single memory 120 rather than a main memory and a cache memory as recited in claim 1.

The Examiner disagrees with the statement and points out that the Delvaux reference makes reference to multiple memory segments which can be used as a main memory and a cache memory as recited in claim 1 (column 3, lines 21-55), (column 8, lines 41 – 63), (column 10, line 56 – column 11, line 27).

On page 13, the applicants state that the Delvaux reference fails to teach the recited control circuit which can write bytes into either of two memories and that can transfer bytes between the two memories as recited in claim 1.

The Examiner disagrees with the statement and points out that the Delvaux reference does teach the recited control circuit which can write bytes into either of two

memories and that can transfer bytes between the two memories as recited in claim 1 (column 12, lines 34-51).

On page 13, the applicants mention although Delvaux's figure 6 shows only a single memory 120, it is divided into two sections, an interleave memory 122 and a "fast path" memory 124. However, the two memory sections 122 and 124 are not similar in purpose to the separate main and cache memories recited in claim 1.

The Examiner disagrees with the statement and points out the Delvaux reference teaches multiple memory elements which can be used for the same purpose, hence the two memory sections 122 and 124 can be similar in purpose to the separate main and cache memories recited in claim 1 (column 3, lines 21-37) and (column 10, line 56 – column 11, line 27).

On page 14, the applicants mention while Delvaux does show two memories (or memory sections) 122 and 124, there is no transfer of data between the two memories 122 and 124 as recited in claim 1. Thus, claim 1 is patentable over Delvaux because Delvaux fails to teach the recited control circuit "for transferring bytes between the main memory and the cache memory" as recited in claim 1.

The Examiner disagrees with the statement and points out that the Delvaux reference does teach "for transferring bytes between the main memory and the cache memory" as recited in claim 1 (column 7, lines 47-62).

On page 14, the applicants mention the Delvaux reference does not discuss read or write accessing a memory in a "burst mode" as recited in claim 3.

The Examiner disagrees with the statement and points out that the Delvaux reference does not discuss read or write accessing a memory in a "burst mode" as recited in claim 3 (column 1, lines 17-24), (column 2, lines 18-40) and (column 2, line 18 – column 3, line 3).

On page 15, the applicants mention the Delvaux reference does not teach to use the recited burst read mode or burst write mode when read or write accessing a main memory while independently accessing individual addresses of a separate cache memory as recited in claim 3.

The Examiner disagrees with the statement and points out the Delvaux reference does teach to use the recited burst read mode or burst write mode when read or write accessing a main memory while independently accessing individual addresses of a separate cache memory as recited in claim 3 (column 1, lines 17-24), (column 2, lines 18-40) and (column 2, line 18 – column 3, line 3).

35 U.S.C. 102 Rejection

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 – 22 are rejected under 35 U.S.C. 102(e) as being unpatentable over Delvaux et al. (U.S. Patent No. 6,971,057).

With respect to claim 1, the Delvaux et al. reference teaches a main memory for storing a plurality of bytes, each at a separate address (column 3, lines 21-37); a cache memory for storing a plurality of bytes, each at a separate address (column 10, line 56 – column 11, line 27); a control circuit for writing bytes of each first word into either the main memory or the cache memory (column 12, lines 34-51); for transferring bytes between the main memory and the cache memory (column 11,

lines 15-21); for reading bytes out of the cache memory or the main memory and forming each second word comprises bytes of more than one of the first words (column 12, line 52 – column 13, line 11), (column 21, lines 1-29).

With respect to claim 2, the Delvaux et al. reference teaches wherein the cache memory And the control circuit are implemented within a single integrated circuit (see Fig. 6), (column 11, line 66 – column 12, line 12); and wherein the main memory is external to the IC (column 12, lines 27-330.

With respect to claim 3, the Delvaux et al. reference teaches wherein the control circuit operates in a burst read mode in which it reads bytes stored at a plurality of sequential addresses of the main memory whenever it read accesses the main memory (column 1, lines 17-22), (column 2, lines 18-40), and column 2, line 41 – column 3, line 7); wherein the control circuit operates in a burst mode in which it writes bytes to a plurality of sequential adresses of the main memory whenever it write accesses the main memory (column 1, lines 17-220, (column 2, lines 18-40) and column 2, line 41 – column 3, line 7); wherein the control circuit independently read and write accesses each individual addrress of the cache memory whenever it reads a byte from or writes a byte to the cache memory (column 11, lines 28-55).

With respect to claim 4, the Delvaux et al. reference teaches wherein the control circuit writes bytes of each first word into the main memory so they are addressed in the main memory in an order in which those bytes appear in the first word (column 12, lines 34 – 40); wherein the control circuit reads bytes out of the main memory and writes them to the cache memory (column 12, lines 40-51); wherein the memory control circuit forms each second word from bytes it reads out of the cache memory (column 14, lines 24 – 46).

With respect to claim 5, the Delvaux et al. reference teaches wherein the control circuit writes bytes of each first word into the cache memory (column 13, lines 6-11); wherein the control circuit reads bytes of the first words out of the cache memory and writes them to the main memory such that they are addressed in the main memory in an order in which they are to appear in the second words (column 14, lines 34-46); and wherein the control circuit forms each second word from bytes it reads out of the cache memory and the main memory (column 11, lines 28-30), (column 14, lines 24-46).

With respect to claim 6, the Delvaux et al. reference teaches an input buffer for receiving and storing bytes forming each first word (column 17, lines 50-55); wherein the control circuit reads bytes forming each first word from the input buffer (column 11, lines 37- 41); and writes them to the main memory so that they are addressed in

the main memory in an order in which the bytes appear in that first word (column 12, lines 34-51); and also reads bytes forming first words out of the input buffer and writes them to the cache memory (column 11, lines 51-55); and an output buffer, wherein the control circuit forms the second words in the output buffer by reading bytes out of the cache memory and writing them into the output buffer (column 11, lines 28-55).

With respect to claim 7, the Delvaux et al. reference teaches an input buffer for receiving and storing each first word (column 17, lines 50-55), wherein the control circuit transfers bytes forming each first word from the input buffer to the cache memory (column 11, lines 51-55); an output buffer, wherein the control circuit forms the second words in the output buffer by reading bytes out of the main memory and out of the cache memory and writing them into the output buffer (column 11, lines 28-55).

With respect to claim 8, the Delvaux et al. reference teaches wherein the control circuit writes every byte of each first word into the main memory (column 11, lines 37-55), (column 14, lines 7-16).

With respect to claim 9, the Delvaux et al. reference teaches wherein the control circuit writes some, but less than all, bytes of each first word into the main memory (column 8, lines 41-63).

With respect to claim 10, the Devlaux et al. reference teaches wherein the control circuit writes every byte of each first word into the main memory (column 11, lines 37-55), 9column 14, lines 7-16).

With respect to claim 11, the Delvaux et al. reference teaches wherein the control circuit writes some, but less than all, bytes of each first word into the main memory (column 8, lines 41-63).

With respect to claim 12, the Devlaux et al. reference teaches writing bytes of each first word into a main memory or into a cache memory (column 13, lines 6-11); transferring bytes between the main memory and the cache memory (column 14, lines 34-46); reading bytes of the cache memory or the min memory and forming each second word from them such that each second word comprises bytes of more than one of the first words (column 12, line 52 – column 13, line 11), (column 21, lines 1-29).

With respect to claim 13, the Devlaux et al. reference teaches wherein a plurality of bytes are read from a plurality of sequential addresses of the main memory in a burst read mode of accessing the main memory whenever the main memory is read accessed (column 1, lines 17-22), (column 2, lines 18-40), and column 2, line 41 – column 3, line 7); wherein the plurality of bytes are written to a plurality of sequential addresses of the main memory in a burst mode whenever the main memory is write accessed column 1, lines 17-220, (column 2, lines 18-40) and column 2, line 41 – column 3, line 7); wherein a single address of the cache memory is independently read or write accessed whenever the cache memory is read or write accessed (column 11, lines 28-55).

With respect to claim 14, the Devlaux et al. reference teaches wherein the step of writing bytes of each first word into the main memory so that they are addressed in the main memory in an order in which those bytes appear in that first word (column 12, lines 34-51); wherein the step of transferring comprises reading bytes out of the main memory and writing them to the cache memory (column 11, lines 51-55); wherein he step of reading comprises forming each second word from bytes read out of the cache memory (column 11, lines 28-55)..

With respect to claim 15, the Delvaux et al. reference teaches wherein the step of writing comprises writing bytes of each first word into the cache memory (column 13,

lines 6-11); wherein the step of transferring comprises reading bytes out of the cache memory and writing them to the main memory (column 14, lines 34-46); and wherein thhe step of reading comprises forming each second word from bytes read out of the cache memory and the main memory (column 11, lines 28-30), (column 14, lines 24-46).

With respect to claim 16, the Delvaux et al. reference teaches storing bytes forming each first word in an input buffer (column 17, lines 50-55); reading bytes of each first word stored in the input buffer and writing them to the main memory (column 11, lines 41-55); reading selected bytes of each first word stored in the input buffer and writing them to selected addresses of the cache memory (column 12, lines 34-51); wherein the step of transferring comprises reading bytes out of the main memory and writing them into a cache memory (column 11, lines 51-55); wherein the step of writing comprises reading bytes forming the second word out of the cache memory and writing them into an output buffer (column 11, lines 28-55).

With respect to claim 17, the Delvaux et al. reference teaches storing bytes forming the first word in an input buffer (column 17, lines 50-55); reading bytes of the first word from the input buffer and writing them to the cache memory (column 11, lines 51-55); wherein the step of transferring comprises reading bytes forming the first word out of the cache memory and writing them to the main memory (column

14, lines 34-46); reading bytes forming the second word out of the main memory and out of the cache memory (column 11, lines 28-30), (column 14, lines 24-46); and writing them into an output buffer to form the second word in the output buffer (column 11, lines 28-55).

With respect to claim 18, the Delvaux et al. reference teaches reading bytes of the step of writing comprises reading all bytes of the first word out of the input buffer and writing them into the main memory (column 11, lines 37-55), (column 14, lines 7-16).

With respect to claim 19, the Delvaux et al. reference teaches reading less than all bytes of the first word out of the input buffer and writing them to the main memory (column 8, lines 41-63).

With respect to claim 20, the Delvaux et al. reference teaches reading all bytes of the first word written into the cache memory back out of the cache memory and writing them to the main memory (column 14, lines 34-46).

With respect to claim 21, the Delvaux et al. reference teaches reading less than all of the bytes of the first word written into the cache memory back out of the cache memory and writing them into the output bufer (column 11, lines 28-55).

With respect to claim 22, the Delvaux et al. reference teaches a first memory for storing a plurality of bytes, each at a separate address (column 3, lines 21-37); a second memory for storing a plurality of bytes, each at a separate address (column 10, line 56 – column 11, line 27); a control circuit, coupled to the first memory and to the second memory, for writing bytes of each first word into the first memory, for transferring bytes between the first memory and the second memory , for reading bytes out of the second memory and forming each second word there from such that each second word comprises bytes of more than one of the first words (column 12, line 52 – column 13, line 11), (column 21, lines 1-29).

Conclusion

1. THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not

mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Enam Ahmed whose telephone number is 571-270-1729. The examiner can normally be reached on Mon-Fri from 8:30 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis-Jacques, can be reached on 571-272-6962.

The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

EA

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11/17/07

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